Key: IEEE JNL = IEEE Journal or Magazine, IEE JNL = IEE Journal or Magazine, IEEE CNF = IEEE Conference, II CNF = IEE Conference, IEEE STD = IEEE Standard

1. **Modeling technology impact on cluster microprocessor performance**
   Codrescu, L.; Nugent, S.; Meindl, J.; Wills, D.S.;
   Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
   Volume 11, Issue 5, Oct. 2003 Page(s):909 - 920
   IEEE JNL

2. **Practical delay enforced multistream (DEMUS) control of deeply pipelined processors**
   McCrackin, D.C.;
   Computers, IEEE Transactions on
   Volume 44, Issue 3, March 1995 Page(s):458 - 462
   IEEE JNL

3. **Improving latency tolerance of multithreading through decoupling**
   Parcerisa, J.-M.; Gonzalez, A.;
   Computers, IEEE Transactions on
   Volume 50, Issue 10, Oct. 2001 Page(s):1084 - 1094
   IEEE JNL

4. **Analytic performance modeling for a spectrum of multithreaded processor architectures**
   Dubey, P.K.; Krishna, A.; Squillante, M.S.;
   Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1995. MASCOTS '95., Proceedings of the Third International Workshop on
   18-20 Jan. 1995 Page(s):110 - 122
   IEEE CNF

5. **Analysis of performance limitations in multithreaded multiprocessor architectures**
   Zuberek, W.M.;
   Application of Concurrency to System Design, 2001. Proceedings. 2001 International Conference on
   25-29 June 2001 Page(s):43 - 52
   IEEE CNF

6. **The shadow algorithm: a scheduling technique for both compiled and interpreted simulation**
   Maurer, P.M.;
   Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
   Volume 12, Issue 9, Sept. 1993 Page(s):1411 - 1413
   IEEE JNL

7. **Hazard pointers: safe memory reclamation for lock-free objects**
   Michael, M.M.;
   Parallel and Distributed Systems, IEEE Transactions on
   Volume 15, Issue 6, June 2004 Page(s):491 - 504
   IEEE JNL

8. **Design experience of a chip multiprocessor Merlot and expectation to functional verification**
   Matsushita, S.;
   System Synthesis, 2002. 15th International Symposium on
   2002 Page(s):103 - 108
   IEEE CNF

9. **Multiple-banked register file architectures**
   Cruz, J.-L.; Gonzalez, A.; Valero, M.; Topham, N.P.;
   Computer Architecture, 2000. Proceedings of the 27th International Symposium on
   2000 Page(s):316 - 325
   IEEE CNF

10. **Impact of implementation on XTP throughput performance**
Saulnier, E.T.; Mitchell, R.J.;
Communications, 1992. ICC 92, Conference record, SUPERCOMM/ICC '92, Discovering a New World of Communications. IEEE International Conference on
14-18 June 1992 Page(s):976 - 980 vol.2

IEEE CNF

11. **Multithreading to improve cycle width and CPI in superpipelined superscalar processors**
Goossens, B.; Duc Thang Vu;
Parallel Architectures, Algorithms, and Networks, 1996. Proceedings. Second International Symposium on
12-14 June 1996 Page(s):36 - 42

IEEE CNF

12. **Design and performance evaluation of a multithreaded architecture**
Govindarajan, R.; Nemawarkar, S.S.; LeNir, P.;
High-Performance Computer Architecture, 1995. Proceedings. First IEEE Symposium on
22-25 Jan. 1995 Page(s):298 - 307

IEEE CNF

13. **The effects of STEF in finely parallel multithreaded processors**
Yamin Li; Wanming Chu;
High-Performance Computer Architecture, 1995. Proceedings. First IEEE Symposium on
22-25 Jan. 1995 Page(s):318 - 325

IEEE CNF

14. **The effects of explicitly parallel mechanisms on the multi-ALU processor cluster pipeline**
Chang, A.; Dally, W.J.; Keckler, S.W.; Carter, N.P.; Lee, W.S.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conference on
5-7 Oct. 1998 Page(s):474 - 481

IEEE CNF

15. **A multithreaded multimedia processor merging on-chip multiprocessors and distributed vector pipelines**
Mombers, F.; Mlynek, D.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on
Volume 4, 30 May-2 June 1999 Page(s):287 - 290 vol.4

IEEE CNF